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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------------|------------------|-------------------------|---------------------|------------------|
| 09/690,634 | 10/17/2000 | Christian Fraisse | \$1022/8429 1622 | |
| 7590 05/06/2004 | | | EXAMINER | |
| James H. Morris | | | JAMAL, ALEXANDER | |
| Wolf, Greenfie | eld & Sacks P.C. | | | |
| Federal Reserve Plaza | | | ART UNIT | PAPËR NUMBËR |
| 600 Atlantic Avenue, | | | 2643 | 0 |
| Boston, MA 02210-2211 | | | | . 8 |
| · | | DATE MAILED: 05/06/2004 | | |

Please find below and/or attached an Office communication concerning this application or proceeding.

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|---|--|--|--|--|--|--|
| • | Application No. | Applicant(s) | | | | |
| | 09/690,634 | FRAISSE ET AL. | | | | |
| Office Action Summary | Examiner | Art Unit | | | | |
| | Alexander Jamal | 2643 | | | | |
| The MAILING DATE of this communication apperiod for Reply | pears on the cover sheet with the c | orrespondence address | | | | |
| A SHORTENED STATUTORY PERIOD FOR REPL THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1. after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a rep - If NO period for reply is specified above, the maximum statutory period - Failure to reply within the set or extended period for reply will, by statut Any reply received by the Office later than three months after the mailin earned patent term adjustment. See 37 CFR 1.704(b). | 136(a). In no event, however, may a reply be timely within the statutory minimum of thirty (30) day will apply and will expire SIX (6) MONTHS from e, cause the application to become ABANDONE | nely filed s will be considered timely. the mailing date of this communication. D (35 U.S.C. § 133). | | | | |
| Status | | | | | | |
| 1)⊠ Responsive to communication(s) filed on <i>Febuary 25, 2004</i> . | | | | | | |
| 2a) This action is FINAL 2b) ∑ This | s action is non-final. | | | | | |
| 3) Since this application is in condition for allowa |)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is | | | | | |
| closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213. | | | | | | |
| Disposition of Claims | | | | | | |
| 4)⊠ Claim(s) <u>1-30</u> is/are pending in the application. | | | | | | |
| 4a) Of the above claim(s) is/are withdrawn from consideration. | | | | | | |
| 5) Claim(s) is/are allowed. | | | | | | |
| 6) Claim(s) <u>1-5,7-18 and 21-28</u> is/are rejected. | | | | | | |
| 7)⊠ Claim(s) <u>6,19,20,29 and 30</u> is/are objected to. | | | | | | |
| 8) Claim(s) are subject to restriction and/o | or election requirement. | | | | | |
| Application Papers | | | | | | |
| 9)☐ The specification is objected to by the Examine | er. | | | | | |
| 10)⊠ The drawing(s) filed on <u>Febuary 25,2004</u> is/are: a)⊠ accepted or b)□ objected to by the Examiner. | | | | | | |
| Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). | | | | | | |
| Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). | | | | | | |
| 11) The oath or declaration is objected to by the E | xaminer. Note the attached Office | Action or form PTO-152. | | | | |
| Priority under 35 U.S.C. § 119 | | | | | | |
| 12) Acknowledgment is made of a claim for foreign a) All b) Some * c) None of: 1. Certified copies of the priority document 2. Certified copies of the priority document 3. Copies of the certified copies of the priority document application from the International Burea | ts have been received. ts have been received in Applicationity documents have been receive | on No | | | | |
| * See the attached detailed Office action for a list of the certified copies not received. | | | | | | |
| | | | | | | |
| Attachment(s) | | | | | | |
| Notice of References Cited (PTO-892) Notice of Draftsperson's Patent Drawing Review (PTO-948) | 4) Interview Summary | | | | | |
| 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 5) Notice of Informal Patent Application (PTO-152) | | | | | | |
| Paper No(s)/Mail Date | 6) Other: | | | | | |

Art Unit: 2643

DETAILED ACTION

Response to Argument and/or Amendment

- 1. Examiner withdraws objections to the drawings (Figs. 1-5, and 6a).
- 2. Examiner notes that **claims 8-30** have been added to the case.
- 3. Applicant's arguments with respect to claims 1-7 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

- 1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 2. Claims 1-5,7-18,21-28 rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's prior art Figs. 1-5, and further in view of White (6008746).

As per claim 1, applicant's prior art Figs. 1-5 disclose a conventional capacitive isolation barrier in a modem across which a differential clock signal (comprising two complementary signals at the same clock rate) is transmitted (Specification pages 1-3, page 6 line 19 to page 8 line 15) and then regenerated with a divide by two flip-flop and a combination of shaping

Art Unit: 2643

signals. However, applicant's prior art does not disclose using one of the shaping signals to reset the flip-flop.

White discloses a method of recovering a clock signal from noisy or intermittent data. His method will reliably decode Manchester coding, which is widely used in the data industry, in the presence of noise (Col 1 lines 60). He discloses that the clock signal ('Manchester data in' signal in Fig. 2) is pulse shaped to detect the transitions (transition detector 45). The pulse shaped signal M2DAT is fed through counter 75 and the synchronized shaped signal 2XCK is fed to a divide-by-2 flip-flop 105 (Col 3 line 65 to Col 4 line 17). The 2XCK signal (comprising the shaping signal from the transitions of the 'Manchester Data in signal') is also used to reset the flip-flop via the use of sequence counter 402 (Col 7 line 53 to Col 8 line 28) (Col 11 lines 8-64). It would have been obvious to one of ordinary skill in the art at the time of this application to use White's clock recovery circuit in the conventional modem with a capacitive isolation barrier of applicant's prior art for the purpose of allowing the modem to effectively recover the clock signal when communicating with the widely used Manchester coding scheme in a noisy environment. In the modem of the applicant's prior art, the Manchester signal would inherently be transmitted differentially (comprise two complementary signals) for the purpose of being transmitted across the isolation barrier of applicant's prior art Fig. 1.

As per claim 4, claim 4 rejected for the same reasons as claim 1. The Clock input of the D-Flip-Flop receives shaping signals that result from filtering the transitions (which comprise the rising edges of two complementary signals) as per applicant's prior art Fig. 5. The reset input of

Art Unit: 2643

the divide-by-2 flip-flop receives the shaping signals via the sequence counter 402 (White: Fig. 2).

As per claim 8, claim 8 rejected for the same reasons as claims 1 and 4. The 'Manchester Data In' Signal of White, when transmitted differentially across the isolation barrier in applicant's prior art would comprise an input for each complementary clock signal (as per applicant's prior art Fig. 2). In White's system the combined pulses (comprising the first and second shaping signals) are output from counter 75 (White: Fig. 2) and through the use of sequence counter 402, the second pulse (after each alternate edge) will reset (set an initial state) the flip-flop (WHITE: Col 8 lines 1-61). Since both positive-negative, and negative-positive transitions of the clock signal (which comprises the two complementary signals) are shaped by the pulse generator, the pulses of each complementary signal will align. As such, the system comprises the means to reset the flip-flop after each rising edge (or alternating edge) of the second signal (when the falling edge being the first shaping pulse received by the counter).

As per claim 21, claim 21 rejected for the same reasons as claims 1,4,8. The flip-flop is coupled to both of the shaping signals (one from each complementary signal transition).

As per claim 2, applicant's prior art Figs. 1-5 disclose regenerating the clock signal downstream a capacitive isolation barrier carrying two complementary signals.

Application/Control Number: 09/690,634 Page 5

Art Unit: 2643

As per claim 3, claim rejected for the same reasons as claims 1 and 8. The output of the flip flop recovers the initial clock signal (an image of one of the complementary portions of the differential signal.

As per claim 5, applicant's prior art Fig. 5 comprises a logic combination of NAND type and uses inverters to preset the shaping signals.

As per claims 7,9,22 claims rejected for the same reasons as claim 1.

As per claims 10,23 claims 10,23 rejected for the same reasons as claim 8.

As per claims 11,24 claim 11,24 rejected for same reasons as claim 8. The signal '2XCK' in White comprises the first and second shaping signals (applicant's prior art Fig. 5). The signal is coupled to the flip-flop reset input via sequence counter 402.

As per claims 12,13,25,26 applicant's prior art Fig. 5 comprises logic to detect an alternate edge of each of the complementary clock signals and output a pulse between each rising edge of the clock signal. The pulses are combined in gate 43.

As per claims 14-18,27,28, applicant's prior art Fig. 5 comprises first and second resistors connected between the complementary signals, and a capacitor coupled between each clock signal and resistor. The logic further comprises a reference voltage between the first and second resistors, a first and second inverter coupled to the first and second capacitors, respectively. The first and second signals (from the first and second inverters) are input into a NAND gate

Allowable Subject Matter

Claims 6,19,20,29,30 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Art Unit: 2643

Page 6

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Jamal whose telephone number is 703-305-3433. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Curtis A Kuntz can be reached on 703-305-4708. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9306 for regular communications and 703-872-9315 for After Final communications.

AJ April 21, 2004

SUPERVISORY PATENT EXAMINER
1010LOGY CENTER 2600